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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/776,101

02/11/2004

Kim C. Hardee

UMI-360

2835

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HOGAN & HARTSON LLP
ONE TABOR CENTER, SUITE 1500
1200 SEVENTEENTH ST
DENVER, CO 80202

EXAMINER

HOANG, HUAN

ART UNIT

PAPER NUMBER

2827

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
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3 MONTHS

04/05/2007

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No. 10/776,101	Applicant(s) HARDEE, KIM C.	
	Examiner Huan Hoang	Art Unit 2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 January 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-15 and 17-27 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-15 and 17-27 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date <u>011007,011107</u> . | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

The Amendment filed on 01/10/07 has been received and entered.

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 1-15 and 17-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Hidaka.

Hidaka discloses a power-gating technique for an integrated circuit device having a Sleep Mode and a circuit having all the steps and elements as recited in claims 1-15 and 17-20 as follows:

providing an output stage (Fig. 19) directly coupled between a substantially constant supply voltage source (32, Vccs) and a substantially constant reference voltage source (34, Vss);
driving a gate terminal of at least one element (PQd, Fig. 19) of said output stage to a level above that of said supply voltage source ($V_{cc} > V_{ccs}$, Fig. 20) or below that of said reference voltage source (V_{ss} to gate of transistor PQc, Fig. 19, $V_{ss} <$

V_{ss} , Fig. 20) in said Sleep Mode of operation (column 25, lines 19-22, lines 29-35 and lines 42-43 and column 72, lines 56-58 and column 78, lines 65-66); wherein said output stage comprises series coupled P-channel and N-channel transistors coupled between said supply voltage source and said reference voltage source (PQb, NQc, PQd and NQd); wherein said gate terminal of said N-channel transistor is driven below said reference voltage level while in said Sleep Mode of operation; wherein said gate of said P-channel transistor is driven above said supply voltage level while in said Sleep Mode of operation.

Response to Arguments

3. Applicant's arguments filed 01/10/2007 have been fully considered but they are not persuasive.

Applicant stated:

“Hidaka teaches an internal circuit node V_{ccs}, which is clearly shows in FIG.19. The actual power supply supply is V_{cc}, which is a normal external power supply having substantially constant voltage level, and is not generated by the circuit itself. In contrast the internal voltage, V_{ccs}, is generated by a P-channel transistor, which is in turn switched by the gate voltage signal designated “Φ”. In effect, the internal voltage V_{ccs} is merely an internal signal node or a power-gated supply line with a varying voltage signal. Evidence of this is given in the immediately adjacent timing diagram of FIG.20, in which V_{ccs} is shown to be a

switched signal an not a "supply voltage source" as claimed."

(REMARKS/ARGUMENTS, page 7, lines 8-16).

In response to the above statement, independent claims 1, 5, 8, 11, 14, 17 and 10 do not recite any external power supply. The supply voltage source does not need to be an external power supply; therefore, and it can be an internal supply voltage source Vccs that is generated from Vcc.

Clearly shown in FIG. 20, in Sleep mode, Vccs and Vss are substantially constant (Standby period only). Therefore, the rejections of claims 1-15 and 17-20 are still proper.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Hidaka (US 2002/0105845) discloses a semiconductor memory device with reduced current consumption in data hold mode.

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any

extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Huan Hoang whose telephone number is (571) 272-1779. The examiner can normally be reached on Tues-Fri 8:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


Huan Hoang
Primary Examiner
Art Unit 2827

HH
3/29/07